In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. – 18. (Canceled)

19. (Original) A capacitor device, comprising:

an insulator filled shallow trench isolation (STI) region comprised with tapered sides, on a semiconductor substrate, wherein a first section of said STI region features a top surface located at a higher level than the top surface of said semiconductor substrate, and wherein a second section of said STI region features a top surfaces recessed below the top surface of said semiconductor substrate exposing an adjacent portion of said semiconductor substrate, wherein said adjacent portion of said semiconductor substrate features a smooth top surface and a tapered side;

an insulator layer lining all surfaces of said insulator filled STI region;

a capacitor dielectric layer on said smooth top surface, and on said tapered side of said portion of semiconductor substrate located adjacent to recessed, said second STI section;

a capacitor region in said semiconductor substrate located underlying said capacitor dielectric layer;

a conductive structure comprised with a first portion located on said capacitor dielectric layer, and with a second portion located on a portion of said first section of said insulator filled

STI region; and

a metal silicide layer located on a top surface of said conductive structure.

20. (Original) The capacitor device of claim 19, wherein said tapered sides of said insulator filled STI region are at an angle between about 70 to 89 ° in relation to a horizontal top surface of said semiconductor substrate.

21. (Original) The capacitor device of claim 19, wherein said insulator layer, lining the surface of said insulator filled STI region, is a silicon oxide layer at a thickness between about 50 to 300 Angstroms.

22. (Original) The capacitor device of claim 19, wherein the depth of recess in said second section of said insulator filled STI region, below the top surface of said first section of said insulator filled STI region, is between about 1000 to 3500 Angstroms.

23. (Original) The capacitor device of claim 19, wherein the insulator in said insulator filled STI region is silicon oxide.

24. (Original) The capacitor device of claim 19, wherein said capacitor region is located either in an N type or P type region.

25. (Original) The capacitor device of claim 19, wherein said capacitor dielectric layer is a silicon dioxide layer, at a thickness between about 10 to 100 Angstroms.

26. (Original) The capacitor device of claim 19, wherein said conductive structure is a doped polysilicon structure.

27. (Original) The capacitor device of claim 19, wherein said metal silicide layer is comprised of either titanium silicide, tantalum silicide, cobalt silicide, nickel silicide or zirconium silicide.